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Part 1 Chassis Description

1. Circuit Function Description
The following figure shows a block diagram of the AA1-A chassis.
1. POWER SUPPLY
The power supply circuit of the AA1-A chassis comprises a primary rectifier smoothing circuit, an oscillation circuit, a control circuit and an output rectifier circuit.
The AC input voltage is rectified at the double or full-wave rectifier smoothing circuit, and an unstable DC voltage is generated at both terminals of the smoothing capacitor C307. The double or full-wave rectifier circuit is built by switching the triac on or off in IC501<STR81145A>. This voltage is supplied to the oscillation circuit, which is composed of a blocking oscillator circuit that switches the switching transistor Q313 ON and OFF.
A square-wave oscillation is generated in the input winding according to operation of the control circuit. A square-wave with amplitude dependent on the turns ratio of the input and output windings is obtained in the output winding. This is rectified in the output rectifier circuit, and the desired DC voltage is produced.

2. IF & DEFLECTION (TDA8361/8362)
The IF output signal from the tuner passes through the SAW filter, and it is inputted into pins 45 and 46 of IC101.
Within the IC, the IF signal passes through the IF amplifier, video detection and video amplifier circuits, and is outputted from pin 7 as a composite video signal.
In the monaural model, this composite video signal passes through the 5.5MHz(B/G)/6.0MHz(I)/6.5MHz(D/K)/4.5MHz(M) sound bandpass filtering circuit, and it is inputted into pin 5 of IC101. In the stereo model, the SIF signal is supplied from pin 14 of IC181<TDA2546A> to pin 5 of IC101 through the sound bandpass circuit for modulation of the main carrier. In the IC101, this sound IF signal passes through the SIF amplifier, FM detector, external audio switch and audio output circuit, and it is then outputted from pin 50 as audio drive signal (Monaural model). In the stereo model, the main audio signal is fed from pin 1 to the stereo controller IC (MC44131PB).
The video signals applied to pins 13 or 15 are separated into vertical- and horizontal-sync. signals respectively by the sync. separator in the IC.
The horizontal oscillator requires no external components and is fully integrated. This oscillator is always running when the start-pin 36 is supplied with 8V, and the horizontal drive signal is outputted from pin 37. VR401 is used for horizontal centring adjustment.
The separated vertical sync. signal from the sync. separation circuit passes through the vertical-separation circuit, and is applied to trigger divider circuit.
The horizontal oscillation pulse and vertical sync. pulse are monitored by the trigger divider circuit to select either the 50Hz or 60Hz system, and automatically adjust the vertical amplitude.
The output signal from the trigger divider triggers the vertical oscillator circuit whose external timing components consist of R402, C401 to pin 42, and the vertical ramp signal is outputted from pin 43. VR451 is for controlling the amount of AC feedback applied to pin 41 for adjustment of the vertical amplitude.

3. VIDEO CHROMA (TDA8361/8362)
The composite video signal output from the pin 7 of IC101, passes through Q122, and the sound traps X124, X125, X126, X127 to reject the sound carrier components, is then supplied to pin 13 through the equalising circuit consisting of Q135, Q132 and Q134. The external video signal from SCART or other AV terminals is supplied to pin 15.
The video signal input to pin 13 or pin 15 is separated into luminance (Y) signal and chroma signal in IC101. These pins are also common to the H/V-sync. separation circuit input already described.
The peaking of Y signal is adjusted by DC voltage on pin 14.("SHARPNESS" control)
The chroma signal is divided into R-Y and B-Y chroma signals, which are demodulated and output from pin 30 (R-Y) and pin 31 (B-Y). These chroma signals pass through the 1H delay line circuit (IC270), and are re-inputted at pin 29 (R-Y) and pin 28 (B-Y). These R-Y/B-Y signals pass through the RGB matrix circuit and the RGB selector circuit of IC101. The internal RGB signals are generated in the RGB matrix circuit and the RGB selector, consisting of linear amplifiers, clamps and selects either the internal RGB signals or the external RGB signals input from pin 22 (R) , pin 23 (G), pin 24 (B). Selection is controlled by the voltage at the RGB switch control (pin 21) and mixed RGB modes are possible since the RGB switching is fast.
The RGB switch also functions as a fast blanking pin by blanking the RGB output stages; here internal and external RGB signals are overruled. The RGB signals for the on-screen display are superimposed onto the selected RGB signals at the base of transistors Q210, Q211 and Q212 respectively. The saturation of colour gain is controlled by the DC voltage of pin 26. ("COLOUR" control) The contrast control voltage present at pin 25, controls the RGB signal gain, and the brightness control voltage present at pin 17, controls DC level of RGB signals. The RGB signals are finally buffered before being presented to the RGB output pins [pin 20 (R), pin 19 (G), pin 18 (B)].

4. AUDIO OUTPUT
4-1 (AN5265)-Monaural model
The audio signal output from pin 50 of IC101 is inputted to pin 2 of IC171 and passes through the pre-amplifier circuit and the drive circuit into the audio amplifier. The audio amplifier is the SEPP (Single-Ended Push Pull) type and the output from pin 8 drives the speaker directly.

4-2 (TDA7263M)-Stereo model
The audio signals output from pins 17 and 18 of IC1101 (MC44131PB) are inputted to pins 1 (Left) and 5 (Right) of IC1102 and passes through the pre-amplifier circuit and drive circuit, after which it is input to the audio amplifier. The audio amplifier is the SEPP (single-ended, push-pull) OTL type and the outputs from pins 8 (Right) and 10 (Left) drive the speakers directly.

5. VERTICAL OUTPUT
An LA7833 is used for the vertical output circuit in this chassis. The vertical ramp signal from pin 43 of IC101 is inputted to pin 4 of IC451. This ramp drives IC451, and vertical scanning is performed. In the first half of scanning a deflecting current is outputted from pin 2 and passes through the following path:
Vcc → pin 2 → pin 1 → VR451/R459 → C461 → DY
Once the magnetic field in DY has dissipated, the current path becomes:
Vcc → pin 6 → pin 7 → C452 → pin 3 → pin 2 →
DY → C461 → VR451/R459 and when the prescribed current value is reached, the vertical drive ramp signal turns ON. This completes one cycle.

6. HORIZONTAL OUTPUT
The horizontal oscillation signal is outputted from pin 37 of IC101 and used to switch the drive transistor Q431. This switching signal is current amplified by the drive transformer T431 and drives the output transistor Q432. When Q432 turns ON, an increasing current flows directly to the DY through
C441/C442 → L441/R441 → DY → Q432-C → Q432-E
and the deflection occurs during the last half of the scanning period. When Q432 turns OFF, the magnetic field stored in the DY up to that point causes a resonant current to flow into the capacitors C420 and C423 and charges them. The current stored in C420 and C423 then flows back to the DY causing an opposite magnetic field to be stored in the DY. This field then collapses increasing a current which switches the dumper diode in Q432 ON. The resonance state is completed, and an increasing current then flows again directly to the DY through the dumper diode.

By this means, the deflection in the first half of the scanning period is performed. When Q432 turns ON at the end of the first half of the scanning period, the deflection during the last half is begun, thus completing one cycle.

In the PCC circuit consisting of Q461 and Q462, the parabola signal supplied from the vertical circuit is added at the horizontal output stage and pincushion compensation is performed by varying the DC bias. Further, the ABL voltage is feedback to the base of Q462 to compensate for width variations due to variations in the beam current.
2. CPU

The following figure shows a block diagram of the CPU peripheral circuit.
The following table shows pin descriptions of the CPU.

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Horizontal sync. signal input</td>
<td>27</td>
<td>+5V power supply</td>
</tr>
<tr>
<td>2</td>
<td>Vertical sync. signal input</td>
<td>28</td>
<td>Oscillator 2 for OSD</td>
</tr>
<tr>
<td>3</td>
<td>Volume control output</td>
<td>29</td>
<td>Oscillator 1 for OSD</td>
</tr>
<tr>
<td>4</td>
<td>Colour control output</td>
<td>30</td>
<td>Reset input</td>
</tr>
<tr>
<td>5</td>
<td>Brightness control output</td>
<td>31</td>
<td>Detection power failure (Error: Lo)</td>
</tr>
<tr>
<td>6</td>
<td>Contrast control output</td>
<td>32</td>
<td>AV2 option switch (Hi: AV2)</td>
</tr>
<tr>
<td>7</td>
<td>Sharpness control output</td>
<td>33</td>
<td>Option switch (System selection)</td>
</tr>
<tr>
<td>8</td>
<td>Tint control output</td>
<td>34</td>
<td>Key scan input (DV)</td>
</tr>
<tr>
<td>9</td>
<td>AV1/AV2 switch output (AV1: Low)</td>
<td>35</td>
<td>Key scan input (DC)</td>
</tr>
<tr>
<td>10</td>
<td>TV/AV switch output (TV: Hi)</td>
<td>36</td>
<td>Option input &amp; SIF output D/K</td>
</tr>
<tr>
<td>11</td>
<td>AFT S-signal input</td>
<td>37</td>
<td>Option input &amp; SIF output I</td>
</tr>
<tr>
<td>12</td>
<td>I²C bus SCL line</td>
<td>38</td>
<td>Option input &amp; SIF output B/G</td>
</tr>
<tr>
<td>13</td>
<td>I²C bus SDA line</td>
<td>39</td>
<td>Option input &amp; SIF output M/M</td>
</tr>
<tr>
<td>14</td>
<td>Tuning voltage output</td>
<td>40</td>
<td>System switch output SECAM</td>
</tr>
<tr>
<td>15</td>
<td>Ident signal input</td>
<td>41</td>
<td>System switch output 3.58</td>
</tr>
<tr>
<td>16</td>
<td>RC signal input</td>
<td>42</td>
<td>System switch output 4.43</td>
</tr>
<tr>
<td>17</td>
<td>---</td>
<td>43</td>
<td>Band switch output I (Low: VH)</td>
</tr>
<tr>
<td>18</td>
<td>Chroma ID input</td>
<td>44</td>
<td>Band switch output II (Low: VL)</td>
</tr>
<tr>
<td>19</td>
<td>Ignore signal input</td>
<td>45</td>
<td>AC switch off detection input</td>
</tr>
<tr>
<td>20</td>
<td>Sync. ID input</td>
<td>46</td>
<td>Option switch (RC status)</td>
</tr>
<tr>
<td>21</td>
<td>---</td>
<td>47</td>
<td>Sound mute output (Mute on: Low)</td>
</tr>
<tr>
<td>22</td>
<td>GND</td>
<td>48</td>
<td>Power on/off output (P-On: Hi)</td>
</tr>
<tr>
<td>23</td>
<td>GND</td>
<td>49</td>
<td>Blanking signal output for OSD</td>
</tr>
<tr>
<td>24</td>
<td>Oscillator input for CPU</td>
<td>50</td>
<td>OSD blue signal output</td>
</tr>
<tr>
<td>25</td>
<td>Oscillator output for CPU</td>
<td>51</td>
<td>OSD green signal output</td>
</tr>
<tr>
<td>26</td>
<td>GND</td>
<td>52</td>
<td>OSD red signal output</td>
</tr>
</tbody>
</table>
2-1 A-D Key Identification Circuit

The key identification circuit used in this chassis uses a switched resistive ladder network in an A-D conversion circuit to generate and send a voltage to the CPU when a key is pressed. The CPU uses this voltage to determine which key was pressed. This resistive circuit eliminates the need for encoder/decoder devices, simplifying design and adding to the reliability of the TV.

The table shows the voltages input to CPU pin 34 and 35, when a given key is pressed.

<table>
<thead>
<tr>
<th>Key</th>
<th>Range of Voltages</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>OFF</td>
<td>less than 0.6V</td>
<td>No Key</td>
</tr>
<tr>
<td>K1</td>
<td>0.6V ~ 1.2V</td>
<td>Pos.+</td>
</tr>
<tr>
<td>K2</td>
<td>1.2V ~ 1.8V</td>
<td>Pos.-</td>
</tr>
<tr>
<td>K3</td>
<td>1.8V ~ 2.4V</td>
<td>Vol. +(Tu Slow)</td>
</tr>
<tr>
<td>K4</td>
<td>2.4V ~ 3.0V</td>
<td>Vol. -(Tu Slow)</td>
</tr>
<tr>
<td>K5</td>
<td>3.0V ~ 3.7V</td>
<td>Function</td>
</tr>
<tr>
<td>K6</td>
<td>3.7V ~ 4.3V</td>
<td>Preset/Memory</td>
</tr>
<tr>
<td>K7</td>
<td>4.3V ~ 4.9V</td>
<td>Colour System</td>
</tr>
<tr>
<td>K8</td>
<td>more than 4.9V</td>
<td>SIF System</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Key</th>
<th>Range of Voltages</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>OFF</td>
<td>less than 0.6V</td>
<td>No Key</td>
</tr>
<tr>
<td>SW</td>
<td>0.6V ~ 1.2V</td>
<td>30 prog. positions</td>
</tr>
<tr>
<td>K9</td>
<td>1.2V ~ 1.8V</td>
<td>TV/AV</td>
</tr>
<tr>
<td>K10</td>
<td>1.8V ~ 2.4V</td>
<td>n/a</td>
</tr>
<tr>
<td>K11</td>
<td>2.4V ~ 3.0V</td>
<td>n/a</td>
</tr>
<tr>
<td>K12</td>
<td>3.0V ~ 3.7V</td>
<td>n/a</td>
</tr>
<tr>
<td>K13</td>
<td>3.7V ~ 4.3V</td>
<td>n/a</td>
</tr>
<tr>
<td>K14</td>
<td>4.3V ~ 4.9V</td>
<td>n/a</td>
</tr>
<tr>
<td>K15</td>
<td>more than 4.9V</td>
<td>n/a</td>
</tr>
</tbody>
</table>

* When the supply voltage is 5.0V.
2-2 Option switches

This chassis uses the option function switches to determine several different specifications of the TV set.

The CPU determines the specification of TV by detecting the voltage level on the following pins.


Pins 36 to 39 also operate as SIF system selection outputs.

**Colour system**

![Colour system diagram]

<table>
<thead>
<tr>
<th>Pin11</th>
<th>Rx</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>0V</td>
<td>open</td>
<td>Test</td>
</tr>
<tr>
<td>0.5V</td>
<td>82k</td>
<td>PAL system</td>
</tr>
<tr>
<td>1.2V</td>
<td>33k</td>
<td>VMT system(PAL-TV, PAL/M-NTST/NTSC-AV)</td>
</tr>
<tr>
<td>1.8V</td>
<td>18k</td>
<td>East Europe system(PAL/N-NTSC/SECAM-TV,AV)</td>
</tr>
<tr>
<td>2.5V</td>
<td>10k</td>
<td>Multi system(PAL/M-NTSC/NTSC/SECAM-TV,AV)</td>
</tr>
<tr>
<td>3.0V</td>
<td>6.8k</td>
<td>China system(PAL/M-NTSC/NTSC-TV,AV)</td>
</tr>
<tr>
<td>3.8V</td>
<td>3.3k</td>
<td>n/a</td>
</tr>
<tr>
<td>4.3V</td>
<td>1.5k</td>
<td>n/a</td>
</tr>
<tr>
<td>4.9V</td>
<td>150</td>
<td>n/a</td>
</tr>
</tbody>
</table>

**SIF system**

![SIF system diagram]

<table>
<thead>
<tr>
<th>SW1</th>
<th>SW2</th>
<th>SW3</th>
<th>SW4</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>on</td>
<td>on</td>
<td>on</td>
<td>on</td>
<td>No SIF system</td>
</tr>
<tr>
<td>on</td>
<td>off</td>
<td>on</td>
<td>off</td>
<td>SIF system e (B/G, D/K)</td>
</tr>
<tr>
<td>off</td>
<td>off</td>
<td>on</td>
<td>on</td>
<td>SIF system d (M/M, B/G)</td>
</tr>
<tr>
<td>off</td>
<td>off</td>
<td>on</td>
<td>off</td>
<td>SIF system c (M/M, B/G, D/K)</td>
</tr>
<tr>
<td>on</td>
<td>off</td>
<td>off</td>
<td>off</td>
<td>SIF system b (B/G, I, D/K)</td>
</tr>
<tr>
<td>off</td>
<td>off</td>
<td>off</td>
<td>off</td>
<td>SIF system a (B/G, D/K, I, M/M)</td>
</tr>
</tbody>
</table>
AV modes

Remote control status

No. of programme position
2-3 System switch output

The outputs from pins 40 to 42 of the CPU select the colour system and the outputs from pins 36 to 39 the SIF system. These outputs drive the colour and SIF system switching circuits. The operation of each switching circuit is shown in the tables below.

### Colour system switching output

<table>
<thead>
<tr>
<th>Colour system</th>
<th>Output pins</th>
<th>Display</th>
</tr>
</thead>
<tbody>
<tr>
<td>Auto</td>
<td>H H L</td>
<td>Auto</td>
</tr>
<tr>
<td>PAL/NTSC4.43</td>
<td>H L L</td>
<td>PAL/NTSC4.43</td>
</tr>
<tr>
<td>SECAM</td>
<td>H L H</td>
<td>SECAM</td>
</tr>
<tr>
<td>NTSC</td>
<td>L H L</td>
<td>NTSC</td>
</tr>
</tbody>
</table>

### SIF system switching output

1. Multi system (SIF system a option)

<table>
<thead>
<tr>
<th>SIF system</th>
<th>Output pins</th>
<th>Display</th>
</tr>
</thead>
<tbody>
<tr>
<td>Auto</td>
<td>* H H H</td>
<td>S1</td>
</tr>
<tr>
<td>B/G-5.5MHz</td>
<td>L H H L</td>
<td>S2</td>
</tr>
<tr>
<td>I-6.0MHz</td>
<td>L L H L</td>
<td>S3</td>
</tr>
<tr>
<td>D/K-6.5MHz</td>
<td>L L L H</td>
<td>S4</td>
</tr>
<tr>
<td>M/M-4.5MHz</td>
<td>H L L L</td>
<td>S5</td>
</tr>
</tbody>
</table>

* It depends on receiving TV system

2. 3 system (SIF system b option)

<table>
<thead>
<tr>
<th>SIF system</th>
<th>Output pins</th>
<th>Display</th>
</tr>
</thead>
<tbody>
<tr>
<td>Auto</td>
<td>input H H H</td>
<td>S1</td>
</tr>
<tr>
<td>B/G-5.5MHz</td>
<td>input H L L</td>
<td>S2</td>
</tr>
<tr>
<td>I-6.0MHz</td>
<td>input L H L</td>
<td>S3</td>
</tr>
<tr>
<td>D/K-6.5MHz</td>
<td>input L L H</td>
<td>S4</td>
</tr>
</tbody>
</table>

3. China, PX (SIF system c option)

<table>
<thead>
<tr>
<th>SIF system</th>
<th>Output pins</th>
<th>Display</th>
</tr>
</thead>
<tbody>
<tr>
<td>Auto</td>
<td>* H input H</td>
<td>S1</td>
</tr>
<tr>
<td>B/H-5.5MHz</td>
<td>L H input L</td>
<td>S2</td>
</tr>
<tr>
<td>D/K-6.5MHz</td>
<td>L L input H</td>
<td>S3</td>
</tr>
<tr>
<td>M/M-4.5MHz</td>
<td>H L input L</td>
<td>S4</td>
</tr>
</tbody>
</table>

* It depends on receiving TV system
4. Indonesia (SIF system d option)

<table>
<thead>
<tr>
<th>SIF system</th>
<th>Output pins</th>
<th>Display</th>
</tr>
</thead>
<tbody>
<tr>
<td>Auto</td>
<td>H</td>
<td>input input</td>
</tr>
<tr>
<td>B/G-5.5MHz</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>M/M-4.5MHz</td>
<td>H</td>
<td>L</td>
</tr>
</tbody>
</table>

5. East Europe (SIF system e option)

<table>
<thead>
<tr>
<th>SIF system</th>
<th>Output pins</th>
<th>Display</th>
</tr>
</thead>
<tbody>
<tr>
<td>Auto</td>
<td>H</td>
<td>input input</td>
</tr>
<tr>
<td>B/G-5.5MHz</td>
<td>input H</td>
<td>input H</td>
</tr>
<tr>
<td>D/K-6.5MHz</td>
<td>input L</td>
<td>input H</td>
</tr>
</tbody>
</table>

6. No SIF system

<table>
<thead>
<tr>
<th>SIF system</th>
<th>Output pins</th>
<th>Display</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>input input input input</td>
<td></td>
</tr>
</tbody>
</table>
2-4 Chroma ID

The identification of a colour or black/white broadcast is achieved by sensing the voltage level input at pin 18. This voltage is supplied from pin 26 of IC101 through the inverter circuit, Q771. When there is a black/white broadcast the voltage on pin 26 goes low. Normally, pin 26 operates as colour control function, and the control voltage is from pin 4 of the CPU.

To identify the colour system during a black/white broadcast, the CPU judges that the system is NTSC when the following conditions are detected at same time.

1) The colour system is "AUTO" or "NTSC" system.
2) The field frequency is 60Hz.
3) TV/AV mode is "TV" mode.

2-5 Ident (Identification)

The identification of the receiving signal status is done by the CPU sensing the voltage level at the input pin 15, as shown below. The ident signal is presented at pin 4 of IC101 and fed to pin 15 of the CPU through the converter circuit consisting of Q700, R706 and R722.

When the CPU judges that the system is 4.43MHz, it outputs a "Low" signal from pin 39 to select the PAL/SECAM system.
2-6 Sync. ID

When no signal is received the voltage on pin 14 of IC101 changes to "Low". As a consequence, D783 and Q718 are turned on, and a "High" is supplied to pin 20 of the CPU. As a result, the CPU judges that no signal is being received. In the AV mode, the CPU outputs a "High" signal from pin 51 to drive the blue back function.

<table>
<thead>
<tr>
<th>Pin20</th>
<th>Judgement</th>
</tr>
</thead>
<tbody>
<tr>
<td>L(0~2.0V)</td>
<td>Signal present</td>
</tr>
<tr>
<td>H(4.0 V~5.0V)</td>
<td>No signal</td>
</tr>
</tbody>
</table>

2-7 Bus control

This chassis uses the I²C bus as the interface for operation control between ICs, and the CPU is used as the master for operation control of the Teletext decoder, A2 Stereo decoder, Nicam decoder and Memory IC.

The I²C bus is composed of the SCL(Serial Clock Line) and SDA(Serial Data Line) lines. Data is transmitted over the SDA line in 8-bit units in synchronisation with the SCL line. These lines are also used for the option function. When the TV set turns on, the CPU once sends the slave address of the Teletext IC, Nicam IC and Stereo IC via the SDA line and waits the ACK(Acknowledge) signal from each IC. The CPU judges which decoder is available by receiving the ACK signal.
2-8 Band switching circuit

The band switching control signals are outputted from pins 43 and 44 of the CPU and fed to the base of Q781, Q782 and Q784, band switching transistors. The one of these transistors then outputs the drive voltage (+12V) to the tuner according to output signal as shown below table.

When the UHF band is selected, "High" signal are sent from both pins 43 and 44. The D781 and D782 are cut off, then Q784 and Q783 are turned on and +12V is supplied to UHF terminal on the tuner.

---

---

Band Switching Logic

<table>
<thead>
<tr>
<th>Output</th>
<th>Pin43</th>
<th>Pin44</th>
<th>Q781</th>
<th>Q782</th>
<th>Q783</th>
<th>Selected Band</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin43</td>
<td>Pin44</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>on</td>
<td>off</td>
<td>off</td>
<td></td>
<td>VHF-Low</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>off</td>
<td>on</td>
<td>off</td>
<td></td>
<td>VHF-High</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>off</td>
<td>off</td>
<td>on</td>
<td></td>
<td>UHF</td>
</tr>
</tbody>
</table>
2-9 Tuning and Digital AFT

The tuning system of this chassis also utilises a digital AFT system. In this operation, the tuner is automatically adjusted to the required tuning point of the broadcast signal by increasing and decreasing the tuning voltage within the synchronisation range, whilst checking the 2 signals from the IF/Video decoder IC, IC101 <TDA8361/8362>. The signals which are outputted from pins 4 and 44 of IC101 are fed to pins 15 and 11 of the CPU via the impedance and voltage converter circuit.

The CPU checks the voltage level of the Ident signal at pin 15 and the AFT-S signal at pin 11, and controls the tuning voltage which is supplied to the tuner. The CPU determines that the correct tuning point is achieved when the Ident signal is Hi(5V) and the AFT-S signal is between 2.0V to 3.0V. When the Ident signal is Hi(5V) and AFT-S signal is greater than 3.0V, the CPU judges that the tuning point is incorrect and increases the tuning voltage output from pin 14 of CPU to correct the tuning point.

When the Ident signal is Hi(5V) and AFT-S signal is less than 2.0V, the CPU again judges that the tuning point is incorrect and decreases the tuning voltage output from pin 14 of CPU to correct the tuning point.

The CPU always maintains the correct tuning point by monitoring these two signals.
Input Signal

Pin 11 of IC701
AFT S-Curve Input

Pin 14 of IC701
Tuning Voltage

Pin 15 of IC701
Ident Signal Input

Tuned point

<table>
<thead>
<tr>
<th>Input Voltage Level of Pin 11</th>
<th>Judgement</th>
</tr>
</thead>
<tbody>
<tr>
<td>LL (0V-1.5V)</td>
<td>Tuning Voltage Down</td>
</tr>
<tr>
<td>L (1.5V-2.0V)</td>
<td>Tuning Voltage Down</td>
</tr>
<tr>
<td>M (2.0-2.5V)</td>
<td>Tuned</td>
</tr>
<tr>
<td>H (2.5V-3.0V)</td>
<td>Tuning Voltage Up</td>
</tr>
<tr>
<td>HH (3.5V-5V)</td>
<td>Tuning Voltage Up</td>
</tr>
</tbody>
</table>
2-10 Power On/Stand-by and Protection circuit

1. Power On/Stand-by
   The power on/stand-by signal is outputted from pin 48 of CPU. When the stand-by mode is selected the voltage of pin 48 changes from Hi(5V) to Low(0V), which turns Q792 off and Q793 on. Q793 drives the photo-coupler D315 which in turn drives Q312 on. Finally Q312 stops the oscillation of power circuit switching the TV into the stand-by condition.
   At the same time, Q793 drives the LED, D1120 to illuminate and indicate the stand-by mode.

2. Protection circuit
   A protection circuit is provided to protect the TV set in case of a circuit malfunction. When an abnormality occurs during TV reception it causes pin 31 of the CPU to go continually Low (less than 2.0V). After one second, the CPU detects that a power failure has occurred on the TV set, and the CPU turns the TV into the stand-by condition.
2-11 Horiz./Vert. pulse input

The vertical and horizontal pulse from the deflection circuits are inputted to pins 1 and 2 in order to synchronise the On Screen Display. The vertical pulse inputted to pin 2 is made by the sandcastle pulse which is outputted from pin 38 of IC101. The sandcastle pulse is extracted the horizontal components at the CR integrating circuit consisting of R796 and C791. The horizontal pulse inputted to pin 1 is made by the retrace pulse which is generated on pin 5 of flyback transformer. If one of these pulses is not supplied to the CPU, the on-screen display cannot be displayed.
3. System switches

The following diagram shows the multi system, selection circuit of this chassis. The description on the following page, describe these switches which are controlled by IC701 (CPU) output.
The system switches (S1-S10) are used for multi-standard model. (Refer to the block diagram of system switching circuit on previous page)

S1: Switch for band-limiting on NTSC(3.58) mode (D106)
This switch is driven by ON/OFF signal from CPU (pin39).

S2: Switch for sound carrier trap on NTSC(3.58) mode (D120)
This switch is driven by signal from CPU (pin39).

S3: Switch for sound carrier trap except NTSC(3.58) mode (D121)
This switch is driven by inverting signal from CPU (pin39).

S4: System switch for forced SECAM mode (Q203)
This switch is driven by ON/OFF signal from CPU (pin40).

S5: System switch for forced 4.43 mode (Q222)
This switch is driven by ON/OFF signal from CPU (pin43).
Note: When the colour system is set to "AUTO", both S6 and S7 will turn on.

S6: System switch for forced 3.58 mode (Q221)
This switch is driven by ON/OFF signal from CPU (pin42).

S7: System switch for 4.5MHz filtering on NTSC(3.58) mode (Q152)
This switch is driven by ON/OFF signal from CPU (pin39).

S8: System switch for 5.5MHz filtering on B/G mode (Q154)
This switch is driven by ON/OFF signal from CPU (pin38).

S9: System switch for 6.0MHz filtering on I mode (Q155)
This switch is driven by ON/OFF signal from CPU (pin37).

S10: System switch for 6.5MHz filtering on D/K mode (Q156)
This switch is driven by ON/OFF signal from CPU (pin36).
Note: When the TV system is set to "AUTO", S7, S8, S9 and S10 will turn on.
3-1 Sound Carrier Trap Circuit

When the 4.5MHz system is selected, the CPU outputs a "High" signal from pin 39. Q153 is turned on and Q157 is turned off. As a result D121/D123 are cut off and D120 is turned on. The composite video signal from pin 7 of IC101 is supplied to the base of Q135 via the 4.5MHz trap circuit X125 which removes the intercarrier sound content. From the equalising circuit the CVBS video signal is fed to pin 13 of IC101. When other systems are selected the composite video signal is fed through the 5.5MHz/6.0MHz trap X126, or the 6.5MHz trap X127, which remove the respective intercarrier sound contents. The remaining video is fed to pin 13 of IC101 via the video equalising circuit to compensate the characteristic of video. This switching is shown in the table below.
3-2 SIF Filtering Circuit

In the stereo model, the SIF signal is outputted from pin 14 of IC181 and is supplied to the base of the buffer transistor Q182.

In the monaural model, the video signal which also contains the SIF carrier signal is outputted from pin 7 of IC101 and is supplied to the Q111.

The SIF signal output from Q181 is supplied to pin 5 of IC101 through the sound bandpass filtering circuit. The relevant bandpass filters X151 (4.5MHz), X152 (5.5MHz), X153 (6.0MHz), X154 (6.5MHz) are selected according to the output signals from pins 36 to 39 of the CPU. The SIF signal is then fed via the relevant buffer Q152 (4.5MHz), Q154 (5.5MHz), Q155 (6.0MHz), Q156 (6.5MHz) to the SIF input pin 5 of IC101 for de-modulation.

<table>
<thead>
<tr>
<th>SIF System</th>
<th>Pin 39</th>
<th>Pin 38</th>
<th>Pin 37</th>
<th>Pin 36</th>
<th>Q152</th>
<th>Q154</th>
<th>Q155</th>
<th>Q156</th>
</tr>
</thead>
<tbody>
<tr>
<td>Auto</td>
<td>*</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>*</td>
<td>On</td>
<td>On</td>
<td>On</td>
</tr>
<tr>
<td>5.5MHz</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>Off</td>
<td>On</td>
<td>Off</td>
<td>Off</td>
</tr>
<tr>
<td>6.0MHz</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>Off</td>
<td>Off</td>
<td>On</td>
<td>Off</td>
</tr>
<tr>
<td>6.5MHz</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
<td>On</td>
</tr>
<tr>
<td>4.5MHz</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>On</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
</tr>
</tbody>
</table>

* It depends on receiving system.
3-3 Chroma Crystal Selection

The subcarrier oscillator crystals, X201 for 4.43MHz and X202 for 3.58MHz are used for both colour demodulation and sync. calibration circuits in IC101 (TDA8362).

When the colour system is AUTO, the output signals from pins 42 and 41 of IC701, CPU, are "High", causing Q221 and Q222 to be turned off, and both X201 and X202 are available for oscillation. IC101 identifies the colour subcarrier of the incoming signal and selects the correct crystal oscillator.

When the forced NTSC system is selected, the CPU outputs a "High" from pin 41 and a "Low" from pin 42. Q221 is turned on and Q222 is turned off. As a result, the oscillation of X201 for 4.43MHz is stopped by applying the DC voltage.

For other colour systems using 4.43MHz oscillation in a forced mode, the CPU outputs a "High" from pin 42 and a "Low" from pin 41 which turns Q221 off and Q222 on. The result is that X202 is prevented from oscillating by the application of the DC voltage via Q222.

### Crystal Select

![Crystal Select Diagram]

<table>
<thead>
<tr>
<th>System</th>
<th>Pin 41</th>
<th>Pin 42</th>
<th>Q221</th>
<th>Q222</th>
<th>X201</th>
<th>X202</th>
</tr>
</thead>
<tbody>
<tr>
<td>Auto</td>
<td>H</td>
<td>H</td>
<td>Off</td>
<td>Off</td>
<td>Live</td>
<td>Live</td>
</tr>
<tr>
<td>PAL/NTSC4.43</td>
<td>L</td>
<td>H</td>
<td>Off</td>
<td>On</td>
<td>Live</td>
<td>Dead</td>
</tr>
<tr>
<td>SECAM</td>
<td>L</td>
<td>H</td>
<td>Off</td>
<td>On</td>
<td>Live</td>
<td>Dead</td>
</tr>
<tr>
<td>NTSC</td>
<td>H</td>
<td>L</td>
<td>On</td>
<td>Off</td>
<td>Dead</td>
<td>Live</td>
</tr>
</tbody>
</table>
4. Internal/External source selection

This circuit is for the selection of external AV input source or internal source. The external AV source (AV1 and AV2) are applied to the AV switching IC, IC801. When the AV1 mode is selected, the AV1/AV2 switching signal from pin 9 of the CPU outputs "Low" to pins 9, 10 and 11 to select the AV1 source, and then the video, audio-L and audio-R signals are sent from pins 4, 15 and 14 to the next stage respectively.

In the video signal, the selected external video signal is supplied to pin 15 of IC101 and the internal video signal supplied to pin 13. The selection of internal or external video source is performed in the IC101 by the TV/AV drive signal sending from pin 10 of the CPU via inverter transistor Q202.

In the audio signal, the selected audio signals(L/R) are supplied to the sound control IC, IC1102, MC44131PB, and the selection of external or internal audio source is performed by the bus lines.

The following tables show the TV/AV and AV1/AV2 switching logic output from the CPU.
5. IF/Video/Chroma/Def. Circuit

The following figure shows a block diagram of the IF/Video/Chroma/Def IC peripheral circuits.
6. Audio Circuit

The audio circuit of the AA1-A chassis has been designed for use the following circuits.

(1) Monaural circuit
(2) A2 stereo circuit
(3) A2 stereo and Nicam circuit

6-1 Monaural circuit

The following figure shows a block diagram of the monaural audio peripheral circuits.
6-2 A2 stereo circuit

The following figure shows a block diagram of the A2 stereo audio peripheral circuits.
6-3 A2 stereo and Nicam circuit

The following figure shows a block diagram of the A2 stereo and Nicam audio peripheral circuits.
7. Double/Full-wave rectifier circuit

The rectifier circuit of this chassis is employed the double/full-wave rectifier switching circuit to operate the power supply circuit in stability from 90V to 290V AC input. The fig. 1 shows the double/full-wave rectifier switching circuit using the triac IC STR81145A, IC501.

The triac in the IC501 automatically switches on or off to build up the double or full-wave rectifier circuit according to the input AC voltage level.

In the range from 90V to 145V AC input, the double rectifier circuit is built up by switching the triac on in the IC501 as shown in fig.2. During the positive half cycle of AC input, the current flows as follows; AC(plus) → IC501 pin2 → pin3 → C509 → D509 → AC(minus). The voltage (Vi) is charged in C509. During the negative half cycle, the current flows as follows; AC(minus) → D508 → C508 → IC501 pin3 → pin2 → AC(plus). The voltage (Vi) is charged in C508. As a result, the DC voltage which is double of AC input voltage is observed between the output terminals KG-1 and KG-2.

In the range from 145V to 290V AC input, the full-wave rectifier circuit is build up by switching the triac off as shown in fig.3. During the positive half cycle, the current flows as follows; AC(plus) → D506 → C508/C509 → D509 → AC(minus), and the negative half cycle, AC(minus) → D508 → C508/C509 → D507 → AC(plus). The voltage (Vi) is charged in C508/C509. As a result, the DC voltage which is same level of AC input voltage is observed between the output terminals KG-1 and KG-2. This circuit can be supplied the proper DC voltage to the power oscillation circuit when the AC input voltage varies in the range from 90V to 290V.
Part 2  Block Diagram of ICs

1. TDA8361/8362 <IF/Video/Chroma/Def.>
### Pin description of TDA8361/8362

<table>
<thead>
<tr>
<th>Pin Symbol</th>
<th>Description</th>
<th>Pin Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>AUDEM Audio de-emphasis</td>
<td>27</td>
<td>HUE Hue control input</td>
</tr>
<tr>
<td>2</td>
<td>IFDEM1 IF demodulator tuned circuit</td>
<td>28</td>
<td>BYI B-Y input signal</td>
</tr>
<tr>
<td>3</td>
<td>IFDEM2 IF demodulator tuned circuit</td>
<td>29</td>
<td>RYI R-Y input signal</td>
</tr>
<tr>
<td>4</td>
<td>IDENT Video identification output</td>
<td>30</td>
<td>RYO R-Y output signal</td>
</tr>
<tr>
<td>5</td>
<td>SOIF Sound IF input and volume control</td>
<td>31</td>
<td>BYO B-Y output signal</td>
</tr>
<tr>
<td>6</td>
<td>EXTAU External audio input</td>
<td>32</td>
<td>XTALOUT 4.43MHz output for TDA8395</td>
</tr>
<tr>
<td>7</td>
<td>IFVO IF video output</td>
<td>33</td>
<td>DET Loop filter burst phase detector</td>
</tr>
<tr>
<td>8</td>
<td>DECDIG Decoupling digital supply</td>
<td>34</td>
<td>XTAL1 3.58MHz XTAL connection</td>
</tr>
<tr>
<td>9</td>
<td>GND1 Ground 1</td>
<td>35</td>
<td>XTAL2 4.43MHz XTAL connection</td>
</tr>
<tr>
<td>10</td>
<td>Vp Positive supply voltage(+8V)</td>
<td>36</td>
<td>HOSC Start horizontal oscillator</td>
</tr>
<tr>
<td>11</td>
<td>GND2 Ground 2</td>
<td>37</td>
<td>HOUT Horizontal output</td>
</tr>
<tr>
<td>12</td>
<td>DECF Decoupling filter tuning</td>
<td>38</td>
<td>FBI/SCO Flyback input/sandcastle output</td>
</tr>
<tr>
<td>13</td>
<td>CVBSINT Internal CVBS input</td>
<td>39</td>
<td>PH2LF Phase 2 loop filter</td>
</tr>
<tr>
<td>14</td>
<td>PEAKIN Peaking control input</td>
<td>40</td>
<td>PH1LF Phase 1 loop filter</td>
</tr>
<tr>
<td>15</td>
<td>CVBSEXT External CVBS input</td>
<td>41</td>
<td>VFB Vertical feedback input</td>
</tr>
<tr>
<td>16</td>
<td>CHROMA Chrominance and AV switch input</td>
<td>42</td>
<td>VRAMP Vertical ramp generator</td>
</tr>
<tr>
<td>17</td>
<td>BRI Brightness control input</td>
<td>43</td>
<td>VOUT Vertical output</td>
</tr>
<tr>
<td>18</td>
<td>BO B output</td>
<td>44</td>
<td>AFCOUT AFC output</td>
</tr>
<tr>
<td>19</td>
<td>GO G output</td>
<td>45</td>
<td>IFIN1 IF input 1</td>
</tr>
<tr>
<td>20</td>
<td>RO R output</td>
<td>46</td>
<td>IFIN2 IF input 2</td>
</tr>
<tr>
<td>21</td>
<td>RGBIN RGB insertion and blanking input</td>
<td>47</td>
<td>AGCOUT Tuner AGC output</td>
</tr>
<tr>
<td>22</td>
<td>RI R input</td>
<td>48</td>
<td>DECGAC AGC decoupling capacitor</td>
</tr>
<tr>
<td>23</td>
<td>GI G input</td>
<td>49</td>
<td>TUNEADJ Tuner take-over adjustment</td>
</tr>
<tr>
<td>24</td>
<td>BI B input</td>
<td>50</td>
<td>AOUT Audio output</td>
</tr>
<tr>
<td>25</td>
<td>CON Contrast control input</td>
<td>51</td>
<td>DECDG Decoupling sound demodulator</td>
</tr>
<tr>
<td>26</td>
<td>SAT Saturation control input</td>
<td>52</td>
<td>DECB Decoupling bandgap supply</td>
</tr>
</tbody>
</table>

### 2. TDA4661 <1H Delay Line>

![TDA4661 1H Delay Line Diagram]

- Colour-difference input signals
- Analogue supply
- Sandcastle pulse input
- Pre-amplifiers
- Memory
- Sample and hold
- Addition stages
- Output buffers
- Colour-difference output signals
- Digital supply
- CCO
- Dividers
- 3MHz shifting clock
- TDA4661

---

AA1-A
### Pin description of TDA8204

<table>
<thead>
<tr>
<th>Pin Symbol</th>
<th>Description</th>
<th>Pin Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GND</td>
<td>Ground</td>
<td>22</td>
</tr>
<tr>
<td>2</td>
<td>DACDR</td>
<td>PWM data output (R)</td>
<td>23</td>
</tr>
<tr>
<td>3</td>
<td>DACDL</td>
<td>PWM data output (L)</td>
<td>24</td>
</tr>
<tr>
<td>4</td>
<td>SERI</td>
<td>Serial bus output</td>
<td>25</td>
</tr>
<tr>
<td>5</td>
<td>VDD</td>
<td>+5V supply voltage</td>
<td>26</td>
</tr>
<tr>
<td>6</td>
<td>RSW</td>
<td>Reserve sound switch (status/control)</td>
<td>27</td>
</tr>
<tr>
<td>7</td>
<td>HA0</td>
<td>Hardware address O</td>
<td>28</td>
</tr>
<tr>
<td>8</td>
<td>TEST0</td>
<td>Test 0</td>
<td>29</td>
</tr>
<tr>
<td>9</td>
<td>US2</td>
<td>User bit 2 input</td>
<td>30</td>
</tr>
<tr>
<td>10</td>
<td>US1</td>
<td>User bit 1 output</td>
<td>31</td>
</tr>
<tr>
<td>11</td>
<td>US0</td>
<td>User bit 0 output</td>
<td>32</td>
</tr>
<tr>
<td>12</td>
<td>SCL</td>
<td>Serial clock I²C bus</td>
<td>33</td>
</tr>
<tr>
<td>13</td>
<td>SDA</td>
<td>Serial data I²C bus</td>
<td>34</td>
</tr>
<tr>
<td>14</td>
<td>SD</td>
<td>Serial data I²C bus</td>
<td>35</td>
</tr>
<tr>
<td>15</td>
<td>SCK</td>
<td>Serial clock I²C bus</td>
<td>36</td>
</tr>
<tr>
<td>16</td>
<td>WS</td>
<td>Word select I²C bus</td>
<td>37</td>
</tr>
<tr>
<td>17</td>
<td>VDD</td>
<td>+5V supply voltage</td>
<td>38</td>
</tr>
<tr>
<td>18</td>
<td>C4</td>
<td>Application control bit 4 flag</td>
<td>39</td>
</tr>
<tr>
<td>19</td>
<td>C3</td>
<td>Application control bit 3 flag</td>
<td>40</td>
</tr>
<tr>
<td>20</td>
<td>C2</td>
<td>Application control bit 2 flag</td>
<td>41</td>
</tr>
<tr>
<td>21</td>
<td>C1</td>
<td>Application control bit 1 flag</td>
<td>42</td>
</tr>
</tbody>
</table>
# 8. TDA8205 <NICAM QPSK Demodulator>

![Diagram of TDA8205](image)

## Pin description of TDA8205

<table>
<thead>
<tr>
<th>Pin Symbol</th>
<th>Description</th>
<th>Pin Symbol</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>1 AGND1</td>
<td>Analogue ground 1</td>
<td>22 CK728</td>
<td>728kHz clock input</td>
</tr>
<tr>
<td>2 MC1</td>
<td>Option, 13.104MHz Xtal</td>
<td>23 NDO</td>
<td>NICAM data output</td>
</tr>
<tr>
<td>3 MC2</td>
<td>Option, 11.7MHz Xtal</td>
<td>24 TEST</td>
<td>Test</td>
</tr>
<tr>
<td>4 DF2</td>
<td>Data filter 2 (eye monitor)</td>
<td>25 MMO</td>
<td>Matrix mute output</td>
</tr>
<tr>
<td>5 DF1</td>
<td>Data filter 2 (eye monitor)</td>
<td>26 AGND2</td>
<td>Analogue ground 2</td>
</tr>
<tr>
<td>6 BGin</td>
<td>System BG input</td>
<td>27 ADL</td>
<td>Audio output (left)</td>
</tr>
<tr>
<td>7 In</td>
<td>System I input</td>
<td>28 ADR</td>
<td>Audio output (right)</td>
</tr>
<tr>
<td>8 AGC</td>
<td>AGC filter condenser</td>
<td>29 DC1</td>
<td>De-coupling 1</td>
</tr>
<tr>
<td>9 Vcc2</td>
<td>+12V supply voltage</td>
<td>30 DC2</td>
<td>De-coupling 2</td>
</tr>
<tr>
<td>10 VDD</td>
<td>+5V supply voltage</td>
<td>31 AMOL</td>
<td>Audio mute output (left)</td>
</tr>
<tr>
<td>11 LFIL1</td>
<td>Filter 1 left (J-17 de-emphasis)</td>
<td>32 AMOR</td>
<td>Audio mute output (right)</td>
</tr>
<tr>
<td>12 RG</td>
<td>Gain adjust resistor (DAC)</td>
<td>33 CAP</td>
<td>De-coupling condenser</td>
</tr>
<tr>
<td>13 AGND3</td>
<td>Analogue ground 3</td>
<td>34 MAI</td>
<td>Monaural audio input</td>
</tr>
<tr>
<td>14 RFIL1</td>
<td>Filter 1 right (J-17 de-emphasis)</td>
<td>35 SAIL</td>
<td>Stereo audio input (left)</td>
</tr>
<tr>
<td>15 RESET</td>
<td>Reset</td>
<td>36 SAI/R</td>
<td>Stereo audio input (right)</td>
</tr>
<tr>
<td>16 Vdd</td>
<td>+5V supply voltage</td>
<td>37 EAIL</td>
<td>External audio input (left)</td>
</tr>
<tr>
<td>17 SERI</td>
<td>Serial bus input</td>
<td>38 EAI/R</td>
<td>External audio input (right)</td>
</tr>
<tr>
<td>18 DACDL</td>
<td>DAC data input (left)</td>
<td>39 Vcc1</td>
<td>+12V supply voltage</td>
</tr>
<tr>
<td>19 DACDR</td>
<td>DAC data input (Right)</td>
<td>40 Xk1</td>
<td>11.648MHz Xtal</td>
</tr>
<tr>
<td>20 DGND</td>
<td>Digital ground</td>
<td>41 LF2</td>
<td>Loop filter 2</td>
</tr>
<tr>
<td>21 CK11648</td>
<td>11.648MHz clock output</td>
<td>42 LF2</td>
<td>Loop filter 1</td>
</tr>
</tbody>
</table>
9. TDA7263M <Audio Output>

10. STR81145A <Double/Full-wave Rectifier Switch>
## Part 3 Trouble Shooting Chart

<table>
<thead>
<tr>
<th>Common startpoint</th>
<th>Chassis Series AA1-A</th>
</tr>
</thead>
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<td>Page 41-44</td>
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<tr>
<td>No picture/No sound</td>
<td>Page 45</td>
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<tr>
<td>No picture-sound OK</td>
<td>Page 46</td>
</tr>
<tr>
<td>No sound-picture OK (Stereo model)</td>
<td>Page 47-48</td>
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<tr>
<td>No sound-picture OK (Monaural model)</td>
<td>Page 49</td>
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<tr>
<td>No colour</td>
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<tr>
<td>Incorrect colour phase</td>
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<tr>
<td>No vertical deflection</td>
<td>Page 52</td>
</tr>
</tbody>
</table>
Trouble Shooting Chart

Startpoint symptom: Dead

Dead

Is the fuse OK?

Yes

Check voltage on both ends of C307

250V-400V

Check voltage on both ends of C521

10V-20V

Check voltage on pin 27 of IC701

+5V

Observe voltage B2(+24V) on both ends of C365 when turning on TV set with RC transmitter. The voltage rise up to 10V-24V once and then fall down to 0V immediately.

Yes

It operates protection circuit

No

Check Power primary circuit Q313, Q312, L312, D311, D315, PS501, R503, D501, IC501, C501, C502, C307, C315


Check Power primary circuit T501, D521-D524, C521

Check Power primary circuit IC701, Q521, R523, D526, C522, C729, C721, C722, A1101, L703

Check Power primary circuit Q313, Q312, Q311, C317, R324, R320, R321, R322, T311, D315, C314, R319

Check stand-by circuit Q792, Q793, D361, R792, IC701

Go to next page
Trouble Shooting Chart

Startpoint symptom: Dead

Connect power failure detection diodes, D362, D393, D433, D468, D486

Caution:
Do not keep TV set on more than 5 seconds during the following check otherwise the TV set may have damage.

keep disconnection and check as follow

Check voltage on pin 31 of IC101

5V

Check voltage on Q353-collector

10V-40V

Check voltage B1(+140V) on both ends of C361

80V or more

Check voltage B2(+24V) on terminal "KAA-3"

24V

Check voltage B4(+24V) on pin 6 of IC451

24V

Go to next page
Trouble Shooting Chart

Startpoint symptom: Dead

Check voltage B5(+15V) on pin 1 of IC351

15V

Check voltage B6(+12V) on pin 3 of IC351

12V

Check voltage B7(+8V) on pin 3 of IC352

8V

Check waveform on pin 37 of IC101

Yes

Check waveform on Q431-collector

No

Check voltage on both ends of C421

5V or more

Go to next page

Short circuit on B5 line IC351, D354, C364, R360

Short circuit on B6 line IC351, C371, IC181, A101, IC801, IC1103, C101, C114, C117, C180, C190, C733, C801, C1172

Short circuit on B7 line IC352, IC101, IC280, R368, C372, C407, C406, C137, C136, D215, C283, C282

IC101, D214, R408, R409, X201, X202

Q431, R431, C431, C432, C434, R434, T431

Check horizontal output circuit Q432, L431, C420, R422, DY, C421, D432, R449
Trouble Shooting Chart

Startpoint symptom: Dead

Check voltage on both ends of C469

5V or less → Check CRT heater circuit T471, R481, R475, D467, C469

10V or more → Check voltage on terminal "KB-1"

0V → D485, C488, R485, T471

180V → R476, D363, R776
Trouble Shooting Chart

Startpoint symptom: No picture/No sound

- No picture/No sound
- Is CRT heater lighting?
  - Yes
    - Check voltage (+33V) on both ends of D704
      - 33V
  - No
    - Go to chart "Dead"
- Is supply voltage (+12V) observed on terminal LB, HB, UB on tuner
  - Yes
    - Check AGC voltage on terminal AGC on tuner
      - 3V-6V
  - No
    - Check tuning circuit IC701, C745, L702, R758, Q711, L706, R765, R763, R704, R705, C707, C708, C105, X701, R755, R756, R744, R746, C716, C781, C782, L705
- Is tuning voltage changing on terminal TU on tuner when tuning
  - Yes 0V to 33V
    - Check voltage (+33V) on both ends of D704
      - 33V
  - No
    - Check tuning circuit IC701, C745, L702, R758, Q711, L706, R765, R763, R704, R705, C707, C708, C105, X701, R755, R756, R744, R746, C716, C781, C782, L705
- Is supply voltage (+12V) observed on terminal LB, HB, UB on tuner
  - Yes
    - Check AGC voltage on terminal AGC on tuner
      - 3V-6V
  - No
    - Check voltage on pin 49 of IC101
      - 3V-6V
    - Check tuner and IF peripheral circuit IC101, A101, Q101, R103, C115, T121, L121, C129, C119, X101
    - Check voltage on pin 49 of IC101
      - 0V or 8V
    - Check AGC voltage on terminal AGC on tuner
      - 0V or 8V
    - Check voltage on pin 49 of IC101
      - 3V-6V
    - Check tuner and IF peripheral circuit IC101, A101, Q101, R103, C115, T121, L121, C129, C119, X101
- Check AGC voltage on terminal AGC on tuner
  - 0V or 8V
    - Check voltage on pin 49 of IC101
      - 3V-6V
    - Check tuner and IF peripheral circuit IC101, A101, Q101, R103, C115, T121, L121, C129, C119, X101
    - Check voltage on pin 49 of IC101
      - 0V or 8V
    - Check AGC voltage on terminal AGC on tuner
      - 0V or 8V
    - Check voltage on pin 49 of IC101
      - 3V-6V
    - Check tuner and IF peripheral circuit IC101, A101, Q101, R103, C115, T121, L121, C129, C119, X101
Trouble Shooting Chart

Startpoint symptom: No picture-sound OK

No picture-sound OK

Is video signal observed on Q122-emitter

Yes

Is video signal observed on Q135-base

Yes

Is video signal observed on Q134-base

Yes

Is video signal observed on pin 13 of IC101

Yes

Check voltage on pin 16 of IC101

8V

Q202, R213, R710

0V

Check voltage on pin 17 of IC101

3V-7V

C206, C712, R721, R718

0V

Check voltage on pin 25 of IC101

3V-7V

R231, R232, C1792, R1792, R1794, C1795, R1797

No

IC101, Q122, R134, R137

Check sound trap circuit

R143, D120-D123, R138, R139, L125, L126, X124-X127, R148, R149

Q135, Q134, Q132, R144, R140, R142, R151, R152, L136, C145, C147

C216, R219, SW220, R245, Q134

No

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Trouble Shooting Chart

Startpoint symptom: No sound-picture OK
(Stereo model)

No sound-picture OK
(Stereo Model)

Select correct sound system

NG

No sound on Nicam broadcast

Yes
Check Nicam decoder peripheral circuit
IC541, IC542, Q181, R568, R569, IC543

No sound on A2 stereo broadcast

Yes
Check A2 stereo decoder peripheral circuit
IC1103, R1172, R1176, R1177

No sound on all of broadcasts

Check voltage on pin 15 of IC701

0V
IC101, C132, R767, C718, Q700, R706

4V-5V

Check voltage on pin 45 of IC701

0V
D528, R526, C523, D527

4V-5V

Go to next page
Trouble Shooting Chart

Startpoint symptom: No sound-picture OK
(Stereo model)

- Check voltage on pin 3 of IC1102
  - 11V
    - IC701, Q172, R175, R179
  - 0V
    - Check waveform on pin 1 of IC1102
      - Yes
        - Check audio output circuit IC1102, Headphone, speakers
      - No
        - Check waveform on pin 3 of IC1103
          - Yes
            - Check IC1103 peripheral circuit X1171, C1171, C1173, C1187, C1191, C1188, C1189
          - No
            - Check waveform on pin 1 of IC101
              - Yes
                - C1179, R1183, C1183
              - No
                - Check waveform on pin 5 of IC101
                  - Yes
                    - IC101, C122, C123, C138, R125
                  - No
                    - Check waveform on pin 14 of IC181
                      - Yes
                        - SIF circuit peripheral circuit Q102, R108, C182, X180, IC181, C188, C186, T181, T181
                      - No
                        - Check SIF filtering circuit
                          - No sound on 4.5MHz------ Check Q112, Q152, X151, Q153, Q157 peripheral circuit
                          - No sound on 5.5MHz------ Check Q113, Q154, X152 peripheral circuit
                          - No sound on 6.0MHz------ Check Q113, Q155, X153 peripheral circuit
                          - No sound on 6.5MHz------ Check Q113, Q156, X154 peripheral circuit
                          - All of systems---------- Check Q153, Q157, Q182, R128, C141, C142 peripheral circuit, RB701, IC701
Trouble Shooting Chart

Startpoint symptom: No sound-picture OK
(Monaural model)

No sound-picture OK
(Monaural Model)

Select correct sound system

NG

Check voltage on pin 15 of IC701

4-5V

Check voltage on pin 3 of IC1101

0V

Check voltage on pin 4 of IC1101
when maximum volume setting

6-8V

Check waveform on pin 2 of IC1101

Yes

Check audio output circuit
IC1101, C1116, C1117, C1123, R1129, C1128, R170

No sound-Picture OK
(Monaural Model)

Check waveform on pin 50 of IC101

No

Check SIF filtering circuit
No sound on 4.5MHz------ Check Q112, Q152, X151, Q153, Q157 peripheral circuit
No sound on 5.5MHz------ Check Q113, Q154, X152 peripheral circuit
No sound on 6.0MHz------ Check Q113, Q155, X153 peripheral circuit
No sound on 6.5MHz------ Check Q113, Q156, X154 peripheral circuit
All of systems---------- Check Q111, R150, R111, C143, R116, C122, C123, C128, R125
peripheral circuit
Trouble Shooting Chart

Startpoint symptom: No colour

- No colour
- No colour on NTSC system
  - Yes → Q222, X202
  - No → No colour on PAL/SECAM system
    - Yes → Q221, X201
    - No → No colour on SECAM system
      - Yes → IC280, C284, C285, L285, C281, C280
      - No → No colour on all of systems
        - Check voltage on pin 1 of IC270
          - 5V
          - Check voltage on pin 26 of IC101
            - 2-6V
            - C204, C205, C271, C272, IC101, IC270, R202, C202, C203, R407
    - No → Check voltage on pin 1 of IC270
      - 0V → IC270, C270, D275, C275, R275, L280
      - 2-6V → C204, C205, C271, C272, IC101, IC270, R202, C202, C203, R407
Trouble Shooting Chart

Startpoint symptom: Incorrect colour phase

Incorrect colour phase

Excessive red colour  ➔  Q1761, Q1762, Q210, VR1761, VR1762, D210

Loss or poor red colour  ➔  Q210, R210, D201, R1762, Q1761, Q1762, J1703, VR1761, VR1762, C1761, R1766, R1768

Excessive green colour  ➔  Q1771, Q1772, Q211, VR1772, R1773, D211

Loss or poor green colour  ➔  Q211, R211, D202, R1772, Q1771, Q1772, VR1772, C1771, R1776, R1778, J1702

Excessive blue colour  ➔  Q1781, Q1782, Q212, VR1781, VR1782, D212

Loss or poor blue colour  ➔  Q212, R212, D203, R1782, J1716, Q1781, Q1782, R1786, R1788, VR1781, VR1782, C1781

Incorrect colour phase on NTSC system only  ➔  R793, R732, R7233, R737, C715

Incorrect colour phase on all of systems  ➔  IC270, IC280, IC101, C204, C205, C271, C272
Trouble Shooting Chart

Startpoint symptom: No vertical deflection

No vertical deflection

The horizontal line appears on the screen

Check waveform on pin 4 of IC451

Yes

IC451, C452, DY, D471, C461, R459, R455, VR451, C456, R454, R453, R452, C464, SW220

No

IC101, R401, R456, C454, R402, C401, C402, R403

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